WHAT IS CLAIMED IS:

1. A data latch apparatus, comprising:

a first latch for latching a data signal;

a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative;

a save device connected between said first and second latches for transferring said data signal from said first latch to said second latch, said save device including a first transistor having a gate; and

said first latch including a first node for providing said data signal to said save device, said gate connected to said first node.

2. The apparatus of Claim 1, wherein said first latch has a second node for providing said data signal, said save device including a second transistor having a gate connected to said second node.

3. The apparatus of Claim 2, wherein said first and second transistors are connected at a common node other than said first and second nodes.

4. The apparatus of Claim 3, wherein said save device includes a third transistor connected to said common node.

5. The apparatus of Claim 4, wherein said third transistor has a gate for receiving a control signal which indicates when to transfer said data signal from said first latch to said second latch.

6. The apparatus of Claim 2, wherein said save device includes third and fourth transistors respectively connected to said first and second transistors.

7. The apparatus of Claim 6, wherein said third and fourth transistors have respective gates for receiving a control signal which indicates when to transfer said data signal from said first latch to said second latch.

8. The apparatus of Claim 6, wherein said first latch includes a first plurality of transistors, each transistor of said first plurality having a gate oxide, said third and fourth transistors having respective gate oxides which are thicker than said gate oxides of said first plurality of transistors.

9. The apparatus of Claim 2, wherein said first latch includes an inverter having an input and an output, and wherein said first node is said inverter input and said second node is said inverter output.

10. The apparatus of Claim 2, wherein said first latch includes a first plurality of transistors, each transistor of said first plurality having a gate oxide, said first and second transistors having respective gate oxides which are thicker than said gate oxides of said first plurality of transistors.

11. The apparatus of Claim 1, wherein said second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom.

12. The apparatus of Claim 1, wherein said first latch includes a plurality of transistors having respective gate oxides, said first transistor having a gate oxide that is thicker than said gate oxides of said plurality of transistors.

13. A data processing apparatus, comprising:

data processing logic for performing data processing operations;

a plurality of registers coupled to said data processing logic for storing data associated with said data processing operations, each said register including a plurality of data latch structures; and

each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is

inoperative, and a save device connected between said first and second latches for transferring said data signal from said first latch to said second latch, said save device including a first transistor having a gate, said first latch including a node for providing said data signal to said save device, said gate connected to said node.

14. The apparatus of Claim 13, provided as one of a microprocessor, a microcontroller and a digital signal processor.

15. A wireless communication apparatus, comprising:

an antenna structure for permitting communication via an air interface;

a digital data processor for performing digital data processing operations;

a wireless communication interface coupled between said antenna structure and said digital data processor for interfacing between said antenna structure and said digital data processor; and

said digital data processor including a plurality of data latch structures, each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and a save device connected between said first and second latches for transferring said data signal from said first latch to said second latch, said save device including a first transistor having a gate, said

first latch including a node for providing said data signal to said save device, said gate connected to said node.

16. The apparatus of Claim 15, provided as one of a mobile telephone, a laptop computer and a personal digital assistant.

17. A data latch apparatus, comprising:

a first latch for latching a data signal;

a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative;

a restore device connected between said first and second latches, said restore device having an input for receiving a restore signal, said restore device responsive to said restore signal for transferring said data signal from said second latch to said first latch; and

said restore device further for isolating said second latch from said first latch independently of said restore signal while said first latch is inoperative.

18. The apparatus of Claim 17, wherein said second latch has a first node for providing said data signal to said restore device, said restore device including a first transistor having a gate connected to said first node.

19. The apparatus of Claim 18, wherein said first latch includes a first plurality of transistors, each transistor of said first plurality having a gate oxide, and wherein said first transistor has a gate oxide that is thicker than said gate oxides of said first plurality of transistors.

20. The apparatus of Claim 18, wherein said restore device includes a second transistor having a gate connected to said first node.

21. The apparatus of Claim 20, wherein said first latch includes a first plurality of transistors, each transistor of said first plurality having a gate oxide, said first and second transistors having respective gate oxides which are thicker than said gate oxides of said first plurality of transistors.

22. The apparatus of Claim 20, wherein said restore device includes a third transistor connected in series with said first and second transistors, said third transistor having a gate connected to said input.

23. The apparatus of Claim 22, wherein said restore device includes a fourth transistor connected in series with said first, second and third transistors, said fourth transistor having a gate connected to said input.

24. The apparatus of Claim 23, wherein said input includes a pair of nodes respectively connected to said gates of said third and fourth transistors.

25. The apparatus of Claim 24, wherein said first latch includes a first plurality of transistors, each transistor of said first plurality having a gate oxide, said first and second transistors having gate oxides which are thicker than said gate oxides of said first plurality of transistors, said third and fourth transistors having gate oxides which are thinner than said gate oxides of said first and second transistors.

26. The apparatus of Claim 23, wherein said third and fourth transistors are connected at a common node other than said first node, and wherein said common node provides said data signal to said first latch.

27. The apparatus of Claim 18, wherein said second latch has a second node for providing said data signal to said restore device, said restore device including a second transistor having a gate connected to said second node.

28. The apparatus of Claim 27, wherein said first latch includes a first plurality of transistors, each transistor of said first plurality having a gate oxide, said first and second

transistors having respective gate oxides which are thicker than said gate oxides of said first plurality of transistors.

29. The apparatus of Claim 27, wherein said restore device includes a third transistor connected in series with said first transistor, said third transistor having a gate connected to said input.

30. The apparatus of Claim 29, wherein said restore device includes a fourth transistor connected in series with said second transistor, said fourth transistor having a gate connected to said input.

31. The apparatus of Claim 30, wherein said first latch includes a first plurality of transistors, each transistor of said first plurality having a gate oxide, said first and second transistors having gate oxides which are thicker than said gate oxides of said first plurality of transistors, said third and fourth transistors having gate oxides which are thinner than said gate oxides of said first and second transistors.

32. The apparatus of Claim 30, wherein said restore device includes a fifth transistor connected in series with said first and third transistors, said fifth transistor having a gate connected to said fourth transistor at a third node.

33. The apparatus of Claim 32, wherein said restore device includes a sixth transistor connected in series with said second and fourth transistors, said sixth transistor having a gate connected to said third transistor at a fourth node.

34. The apparatus of Claim 33, wherein said third and fourth nodes provide said data signal to said first latch.

35. The apparatus of Claim 17, wherein said second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom.

36. A data processing apparatus, comprising:

data processing logic for performing data processing operations;

a plurality of registers coupled to said data processing logic for storing data associated with said data processing operations, each said register including a plurality of data latch structures; and

each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and a restore device connected between said first and second latches, said restore device having an input for receiving a restore signal, said restore device responsive to said

restore signal for transferring said data signal from said second latch to said first latch, said restore device further for isolating said second latch from said first latch independently of said restore signal while said first latch is inoperative.

37. The apparatus of Claim 36, provided as one of a microprocessor, a microcontroller and a digital signal processor.

38. The apparatus of Claim 36, including a distribution structure connected to said restore devices for distributing said restore signal to said restore devices, said distribution structure powered by a first power supply, and said second latch powered by a second power supply other than said first power supply.

39. A wireless communication apparatus, comprising:

an antenna structure for permitting communication via an air interface;

a digital data processor for performing digital data processing operations;

a wireless communication interface coupled between said antenna structure and said digital data processor for interfacing between said antenna structure and said digital data processor; and

said digital data processor including a plurality of data latch structures, each said data latch structure including a first latch for latching a data signal, a second latch coupled to said

first latch for retaining said data signal while said first latch is inoperative, and a restore device connected between said first and second latches, said restore device having an input for receiving a restore signal, said restore device responsive to said restore signal for transferring said data signal from said second latch to said first latch, said restore device further for isolating said second latch from said first latch independently of said restore signal while said first latch is inoperative.

40. The apparatus of Claim 39, provided as one of a mobile telephone, a laptop computer and a personal digital assistant.

41. A data latch apparatus , comprising:

a first latch for latching a data signal;

a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative;

a restore device connected between said first and second latches for transferring said data signal from said second latch to said first latch, said restore device further for isolating said second latch from said first latch while said first latch is inoperative; and

said second latch having a first node for providing said data signal to said restore device, said restore device including a first transistor having a gate connected to said first node.

42. The apparatus of Claim 41, wherein said restore device includes a second transistor having a gate connected to said first node.

43. The apparatus of Claim 42, wherein said first latch includes a plurality of transistors, each transistor of said plurality having a gate oxide, said first and second transistors having gate oxides which are thicker than said gate oxides of said plurality of transistors.

44. The apparatus of Claim 43, wherein said restore device includes third and fourth transistors connected in series with said first and second transistors.

45. The apparatus of Claim 44, wherein said third and fourth transistors each have a gate oxide that is thinner than said gate oxides of said first and second transistors.

46. The apparatus of Claim 44, wherein said third and fourth transistors are connected at a common node other than said first node, and wherein said common node provides said data signal to said first latch.

47. The apparatus of Claim 41, wherein said first latch includes a plurality of transistors, each transistor of said plurality having a gate oxide, said first transistor having a gate oxide that is thicker than said gate oxides of said plurality of transistors.

48. The apparatus of Claim 41, wherein said second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom.

49. The apparatus of Claim 41, wherein said second latch has a second node for providing said data signal to said restore device, said restore device including a second transistor having a gate connected to said second node.

50. The apparatus of Claim 49, wherein said first latch includes a plurality of transistors, each transistor of said plurality having a gate oxide, said first and second transistors having gate oxides which are thicker than said gate oxides of said plurality of transistors.

51. The apparatus of Claim 50, wherein said restore device includes third and fourth transistors connected in series with said first and second transistors, respectively, each of said third and fourth transistors having a gate connected to said input.

52. The apparatus of Claim 51, wherein said third and fourth transistors each have a gate oxide that is thinner than said gate oxides of said first and second transistors.

53. The apparatus of Claim 51, wherein said restore device includes a fifth transistor connected in series with said first and third transistors and a sixth transistor connected in series with said second and fourth transistors, wherein said fifth transistor has a gate connected to said fourth transistor at a third node and said sixth transistor has a gate connected to said third transistor at a fourth node, and wherein said third and fourth nodes provide said data signal to said first latch.

54. A data processing apparatus, comprising:

data processing logic for performing data processing operations;

a plurality of registers coupled to said data processing logic for storing data associated with said data processing operations, each said register including a plurality of data latch structures; and

each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and a restore device connected between said first and second latches for transferring said data signal from said second latch to said first latch, said restore device further for isolating said second latch from said first latch while said first latch is inoperative,

said second latch having a first node for providing said data signal to said restore device, said restore device including a first transistor having a gate connected to said first node.

55. The apparatus of Claim 54, provided as one of a microprocessor, a microcontroller and a digital signal processor.

56. A wireless communication apparatus, comprising:

an antenna structure for permitting communication via an air interface;

a digital data processor for performing digital data processing operations;

a wireless communication interface coupled between said antenna structure and said digital data processor for interfacing between said antenna structure and said digital data processor; and

said digital data processor including a plurality of data latch structures, each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and a restore device connected between said first and second latches for transferring said data signal from said second latch to said first latch, said restore device further for isolating said second latch from said first latch while said first latch is inoperative, said second latch having a first node for providing said data signal to said restore device, said restore device including a first transistor having a gate connected to said first node.

57. The apparatus of Claim 56, provided as one of a mobile telephone, a laptop computer and a personal digital assistant.